



Final Project : Dual Sensor Alarm

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Introduction

This experiment involves constructing two sensor circuits: one utilizing a thermistor for heat sensing and the other employing a light-dependent resistor for light sensing. The outputs of these circuits will be linked to an OR gate. When either sensor or both detect their respective inputs, the OR gate will activate a buzzer, turn on a switch that will complete the DC motor circuit simultaneously. This setup will indicate the triggering of one or both sensor circuits.

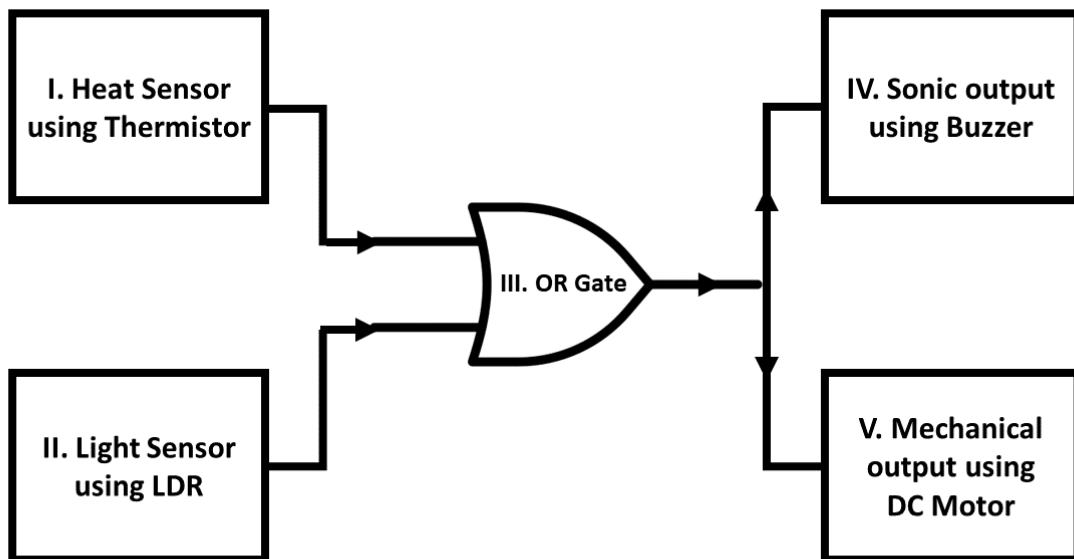


Figure 1: Reference conceptual diagram showing all blocks

Materials & Equipment

- LDR
- 3V Buzzer
- BJT PN2222
- 3V DC Motor
- 14N001 Diodes
- Connecting wires
- DC Power supply
- 3 OpAmp UA741
- 10k Potentiometer
- Function Generator
- NTC Thermistor 10k
- Resistors (1k and 12k)
- MOSFET IC HEF4007
- Solder and Soldering paste

I - Heat Sensor using Thermistor

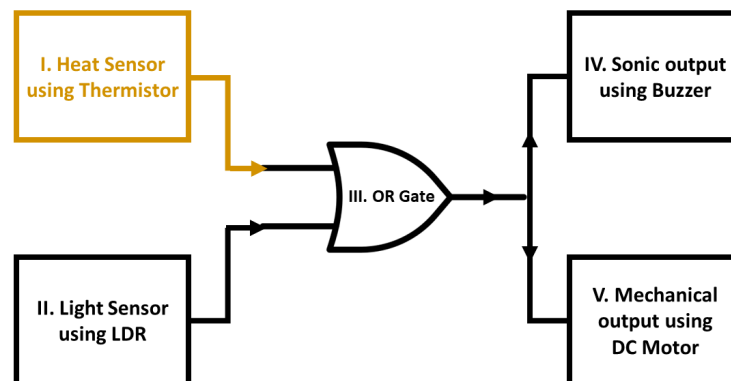


Figure 2: Reference conceptual diagram emphasizing block I

Defining Block I : Functioning of a Heat Sensor

A heat sensor, also known as a thermal sensor or temperature sensor, operates by detecting changes in temperature in its surrounding environment. It typically comprises a sensitive element that responds to variations in temperature by generating an electrical signal proportional to the heat level. This signal is then processed by associated circuitry to provide temperature readings or trigger specific actions such as activating an alarm or controlling a heating or cooling system.

Functioning of the Thermistor

Several types of heat sensors are available, including thermistors. Thermistors, which are temperature-sensitive resistors, undergo changes in resistance corresponding to temperature variations. Two main categories of thermistors exist: Negative Temperature Coefficient (NTC) and Positive Temperature Coefficient (PTC). NTC thermistors demonstrate a decrease in resistance as temperature rises, while PTC thermistors exhibit an increase in resistance with temperature elevation. NTC thermistors are commonly utilized for temperature measurement purposes, whereas PTC thermistors are primarily employed for circuit protection applications. In NTC thermistors, the degree of resistance reduction with temperature escalation isn't consistent but follows a non-linear pattern. Therefore, in this experiment we will be using NTC-10k.

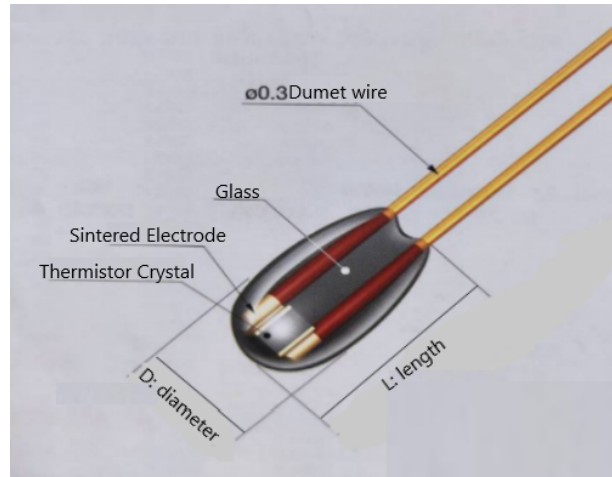


Figure 3: Internal structure of the NTC 10k thermistor

Functioning of a Comparator

As the temperature fluctuates, the resistance of the thermistor alters, affecting the voltage across it according to Ohm's law ($V=RI$). To monitor this voltage change, we employ a voltage comparator utilizing an op-amp. The concept involves setting a reference voltage equivalent to the voltage across the thermistor at room temperature. This reference voltage serves as a constant point of comparison against the varying input voltage of the comparator. When the input voltage surpasses the reference voltage, the output becomes $+V_{CC}$; conversely, if the input voltage falls below the reference, the output switches to $-V_{CC}$.

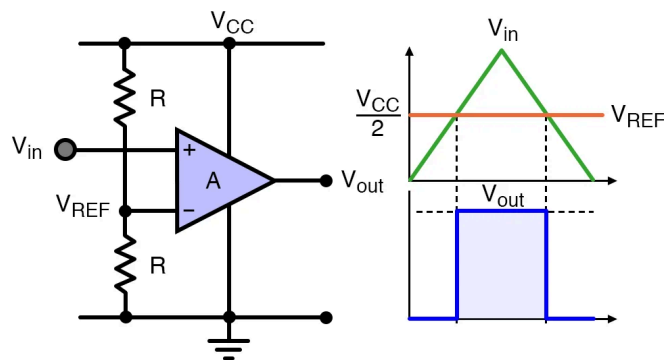


Figure 4: Example comparator configuration for illustration purposes

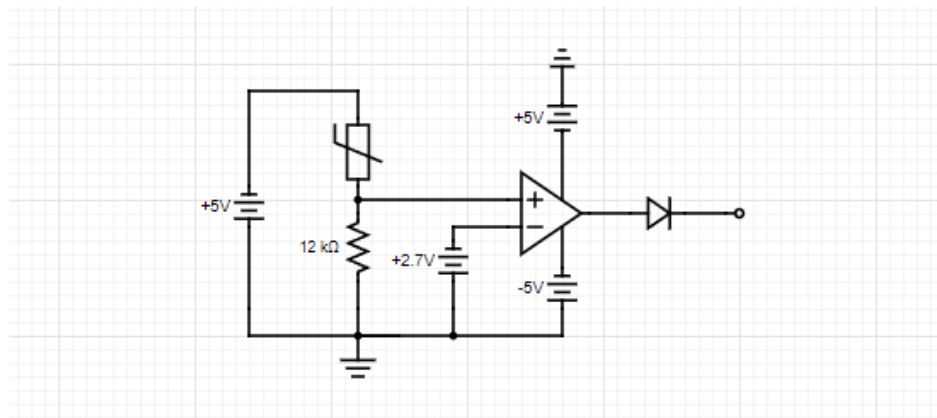
Usage of a Diode at the Output

The diode served to regulate the input of our OR gate. In cases where the output is positive, it becomes forward biased; conversely, when the output is negative, it becomes reverse biased. Its forward biasing causes a voltage drop of approximately 0.7 V, a crucial factor for the circuit's functionality as it reduces the voltage across the buzzer ensuring that the buzzer operates within

safe limits and remains undamaged. On the other hand, when it's reverse bias, it acts as an open circuit, which “clears” the respective input of the OR gate, signaling no significant light changes.

Components used for the Heat Sensor

- Thermistor
- 12kΩ Resistor
- UA741 OpAmp
- 1N4001 Diode
- DC Power Supply / Batteries



We set the DC power supply to produce a 5V output. One terminal of the thermistor was linked to this 5V terminal, while the other terminal was connected to a 12 kΩ resistor, with the second terminal of the resistor going to ground. The junction point between the thermistor and resistor (V_{in}) was connected to the positive input ($V+$) of the op-amp. Additionally, a 2.7V signal from the function generator was connected to the negative input ($V-$) of the op-amp, with its ground tied to the circuit's ground. The $+V_{CC}$ was linked to +5V, while $-V_{CC}$ was connected to -5V obtained from the -25V outlet of the DC power supply. Lastly, a diode's anode was attached to the output, and its cathode served as the input for an OR gate.

Threshold Voltage Calculations for OpAmp

The measured resistance of thermistor at room temperature was 11.3 kΩ .

$$V_{in} = \frac{12}{12 + R_{thermistor}} \times 5 = \frac{12}{12 + 11.3} = 2.5 \text{ V} .$$

When the temperature rises, the resistance of the thermistor drops, causing the voltage across the 12 kΩ resistor to increase. This increase in voltage, above 2.5V, triggers a +5V output, forward biasing the diode and resulting in a high input for the OR gate. Conversely, as the temperature falls, the resistance of the thermistor increases. Consequently, the voltage across the 12 kΩ resistor decreases, falling below 2.5V. This leads to a -5V output, reverse biasing the diode and resulting in a low input for the OR gate.

But when implementing this circuit and choosing the reference voltage, environmental conditions should be taken into account because of the high sensitivity of the op-amp, diode, and the thermistor. Thus, the threshold voltage as well as the voltage across the whole voltage divider need to be tuned to the setting.

Overall Gain, Input and Output Impedances

Gain of the op amp is $G = \frac{V_{out}}{V_{in}}$, and V_{in} is equal to $V_{in} = \frac{12}{12 + R_{thermistor}} \times 5$ as the resistance decreases

$\frac{V_{out}}{V_{in}} = \frac{12}{12 + R_{LDR}}$ increases and the gain will approach 1,

and when the resistance of the this thermistor increases $\frac{V_{out}}{V_{in}} = \frac{1}{1 + R_{LDR}}$, the gain will be negative and will be approaching zero.

Final Detailed Schematic of the Heat Sensor

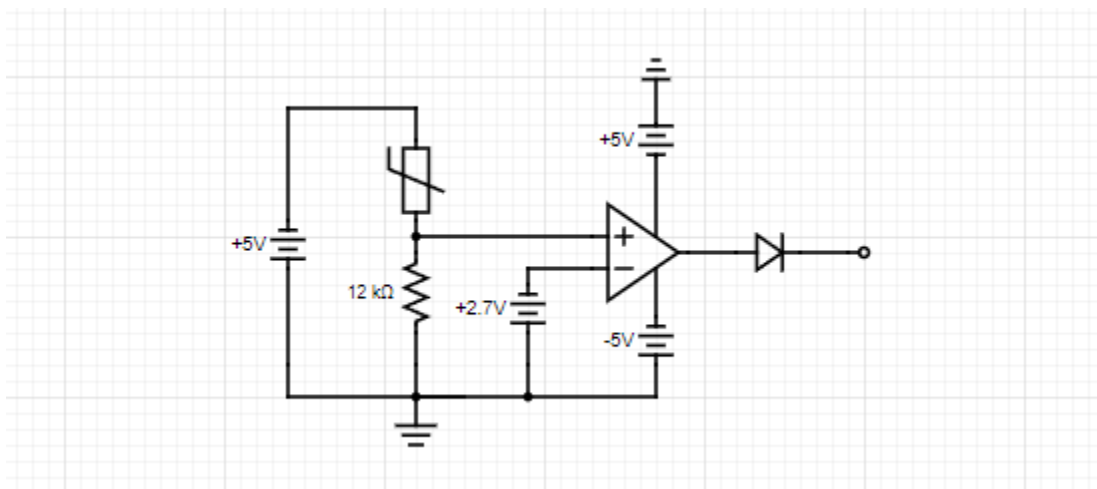


Figure 5: Schematic of the heat sensor using a thermistor

Connections with Rest of the Circuit

The output of this block will serve as one of the inputs for the OR gate that we design in block III.

Issues encountered during Implementation

We first tried to ground Vee, which made the comparator more sensible to the fluctuation of the Thermistor resistance value. We fixed it by applying a $V_{ee} = -V_{cc}$ and then connecting a diode : it provided a null output when the output of the comparator is negative while also providing us with a 0.7 voltage drop when forward bias, which was needed to lower the voltage level before entering the OR gate, in block III, which will be discussed later.

Design Limitation and Optimization Recommendations

The circuit's sensitivity, particularly influenced by the thermistor and op-amp, poses a significant constraint. Even minor fluctuations in the input voltage near the threshold can induce the comparator to switch states due to this heightened sensitivity. This aspect is critical in our scenario as the circuit's resistance varies with room temperature, potentially leading to shifts in the threshold voltage. Managing these variations is essential to ensure consistent performance across diverse environmental conditions.

Furthermore, the inherent imperfections in the op-amp represent another limitation. These imperfections contribute to power consumption and may cause the output voltages to be clipped. Instead of attaining the desired -5V or +5V output, the output voltage may be constrained, impacting the circuit's precision and effectiveness.

Additionally, considering the circuit's variable temperature and the nonlinear nature of a diode's current-voltage characteristic, particularly in the forward bias region, the current also fluctuates.

The voltage across the diode is also given by, $V_d = V_T \ln\left(\frac{I_D}{I_S}\right)$ where,

V_d is the voltage across the diode, V_T is the thermal voltage and it is given by $V_T = \frac{kT}{q}$, I_D is diode current and I_S is the reverse saturation current of the diode.

Hence, as the voltage across the diode is influenced by temperature variations, it further affects the input voltage of the OR gate.

A recommendation for this circuit: measure the room temperature of the circuit and adjust the resistance in series with the thermistor accordingly.

II - Light Sensor using LDR

Now that the first sensor is implemented, we will tackle the second sensor that will give this circuit the ability to detect changes in light using a light-dependent resistor or LDR for short.

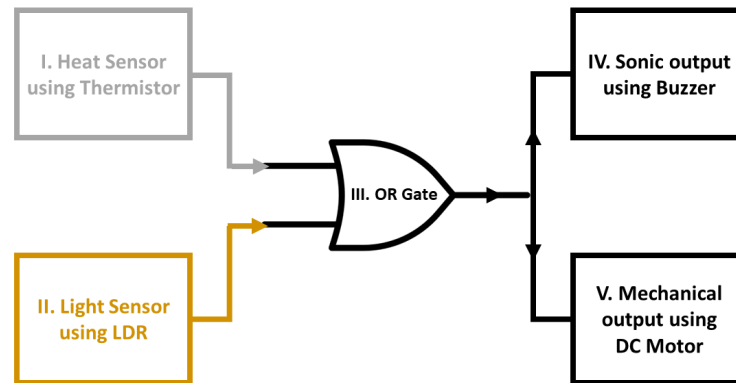


Figure 6: Reference conceptual diagram emphasizing block II

Defining Block II : Functioning of a Light Sensor

A light sensor is a device that detects light and converts it into an electrical signal. Its primary function of a light sensor is to measure the intensity of light in the environment and respond to changes in light conditions. Here, we expect the light sensor's output to go high when an abrupt change in light received from the surface of the LDR is detected, namely, from room light intensity to a shadow or darkness. To achieve this, we will use a LDR.

Structure and Functioning of the LDR

A Light Dependent Resistor (or photoresistor) is a device whose resistance changes when the amount of light its surface receives changes. It is highly useful for sensing light level changes. It is composed of light sensitive semiconductor materials like cadmium sulfide (CdS) or selenide (CdSe)

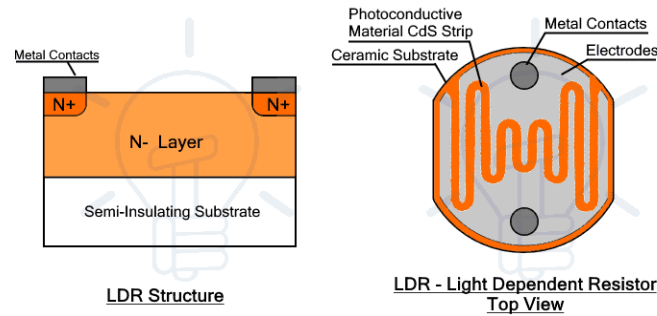


Figure 7: Internal structure of a light dependant resistor (LDR)

Photoconductivity and Resistance of the LDR

It relies on the phenomenon of photoconductivity : when light photons hit the surface of the LDR, they give energy to the electrons in the material. This energy allows the electrons to jump from the valence band of the semiconductor to the conduction band, increasing the number of free charge carriers. As more light is absorbed by the material, more electrons move to the conduction band, thus increasing the electrical conductivity and decreasing the resistance. In the absence of light, the semiconductor has fewer charge carriers, and thus, it exhibits higher resistance.

Usage of the Previous Comparator and Diode Configuration

Using the similar approach of block I, we will rely on the properties of the LDR when connected in series with a resistor in a voltage divider configuration. We connect the junction of this voltage divider to the non-inverting terminal while setting a threshold voltage on the inverting terminal of the open-loop comparator configuration. This way, once the LDR receives light and its resistance starts decreasing, the voltage across the other resistor starts increasing. Once this light intensity received is deemed enough to turn on the alarm, the voltage across the resistor becomes greater than the threshold : the output of the comparator goes high at around V_{cc} with a bit of clipping. Otherwise, its output will be negative (slightly higher than $-V_{cc} = -5$) which would result in the diode at the output being forward biased and thus acts like an open circuit to give a null output.

Threshold Voltage Calculations for Comparator

To calculate the threshold voltage for this circuit we tried to measure the fluctuations of the resistance of the LDR at different lightning conditions.

We observed that with light the resistance of the LDR varies between 1.8 k Ω and 1.4 k Ω and using voltage division and $V_{in} = \frac{1}{1+R_{LDR}} \times 5 = 1.78V \text{ and } 2.083$ respectively.

And when covering the LDR its resistance varied between 36 k Ω and 38.3 k Ω making $V_{in} = 0.13 \text{ V and } 0.127 \text{ V}$ respectively.

And to compensate with the environmental conditions the threshold voltage was chosen to be 1V where the output will be high when the LDR is exposed to light and low when it is covered.

Components used for the Light Sensor

- LDR
- 1k Ω Resistor
- UA741 OpAmp
- 1N4001 Diode
- DC Power Supply
- Batteries (if any)

Overall Gain, Input and Output Impedances of Block II

Gain of the op amp is $G = \frac{V_{out}}{V_{in}}$, and V_{in} is equal to $V_{in} = \frac{1}{1+R_{ldr}} \times 5$ as the resistance decreases

$\frac{V_{out}}{V_{in}} = \frac{1}{1+R_{LDR}}$ increases and with strong light it might exceed 1, And when the resistance of the

this LDR increases $\frac{V_{out}}{V_{in}} = \frac{1}{1+R_{LDR}}$, the gain will be negative and will be approaching zero.

Final Detailed Schematic of Block II

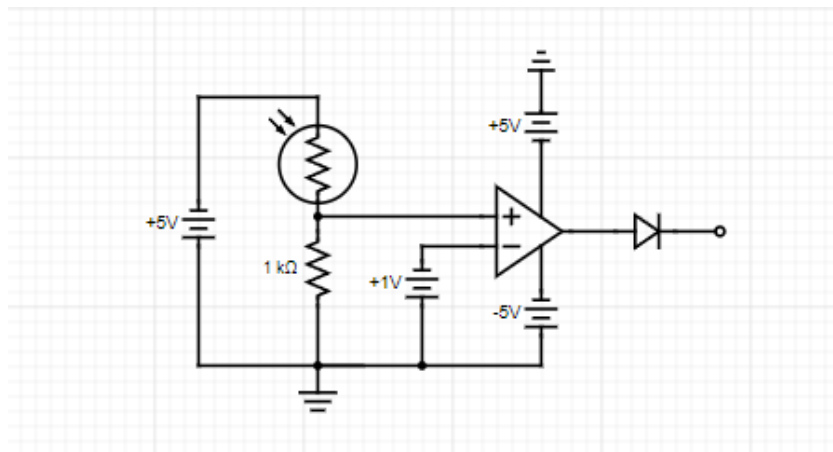


Figure 8: Schematic of the light sensor using the LDR

Connections with Rest of the Circuit

The output of this block will serve as one of the inputs for the OR gate that we design in block III.

Issues encountered during Implementation

Similar issues have been encountered during the implementation of block I and II, including an extra voltage at the output when having Vee grounded instead of being equal to $-V_{cc}$ and not having a diode at the output for a needed voltage drop when the comparator's output is positive and an open circuit resulting in a null output when in reverse bias (negative comparator output).

Design Limitation and Optimization Recommendations

Due to their slow response time and temperature sensitivity, LDRs may not be suitable for high-speed or precise light detection tasks. They also suffer from long-term degradation when exposed to high-intensity light levels.

III - Logic OR Gate

Now that the two sensors are fully functional, with each having an output equal to V_{cc} , we need to connect them to a circuit that signals whether at least one of them is triggered. This can be done using an OR gate.

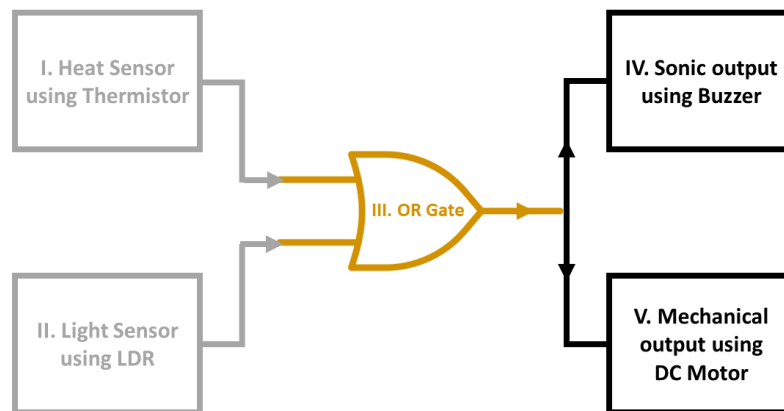


Figure 9: Reference conceptual diagram emphasizing block III

Defining Block III

In logic design, an OR gate is a two-input one-output device whose output goes high if either inputs are high and only goes low when both inputs are simultaneously low. Here is the logic circuit symbol of the OR gate alongside its truth table where A and B are the inputs and C is its output.

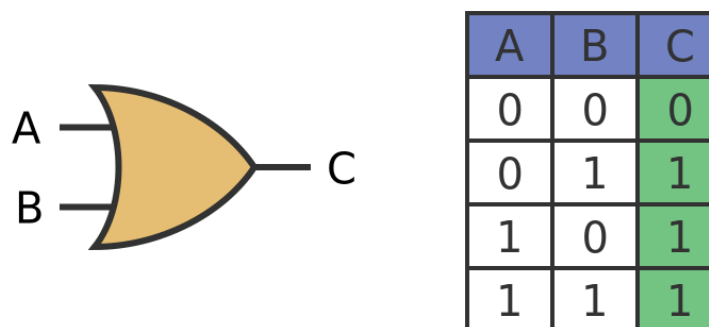


Figure 10: Truth table and symbol of the OR gate

In this design, an input is denoted as high when it's ideally equal to V_{cc} , and low when it's ideally 0V. But given the experimental settings, we need to take fluctuations into consideration. Thus, we will subsequently define a commonly used tolerance interval for what we designate by a logical one

(high) or logical zero (low) value. An output of around 2.7 to 5 volts will be considered as high while an output of 0 to 0.5 is low. If it is greater than the upper bound of the logic-zero's interval but less than the lower bound then the logic-one's interval is considered as a "confused" state that cannot be mapped to a binary value. Our goal is to design this gate in a manner that minimizes the risk of obtaining such values outside of the tolerance intervals of the binary values.

Implementation of the Logic OR Gate

Designing logic gates requires a circuit that has components having some specific properties, such as selectivity and multiple operating modes : this can be roughly done using either diodes or transistors. But in order to efficiently implement a gate, we need to meticulously choose the components involved while also making a compromise between accuracy and complexity. Given the rest of the circuit, our aim is to get enough voltage at the output of the gate in order to turn on the components at the output, namely the buzzer and DC motor already selected to operate on V_{cc} .

Choice of Transistors over Diodes for OR Gate

Diodes already have a voltage drop of around 0.7 when in forward bias, this means that if the input signals are 5V if high and 0 otherwise, the output of the OR gate designed using diodes would be 4.3 V if high, which might not be enough for the rest of the circuit. This voltage drop can be even more significant in digital circuits operating at 3.3 V and lower. Also, they do not have a gain like transistors that can help boost the input signal if needed. That's why we will opt for transistors since they can actively drive the output high or low in a more optimal and efficient manner.

Choice of MOSFETs over Bipolar Junction Transistors

In our design, we will be using MOSFETs instead of BJTs for several reasons : MOSFETs are voltage driven and thus do not need a continuous gate current, unlike transistors that are driven by their base current. This results in a minimization of power consumption and makes them suitable for low-power circuits such as electronics ones. Furthermore, they offer a faster switching speed compared to BJTs because the capacitance at the gate can be charged and discharged quickly. Finally, MOSFETs are more thermally stable than BJTs as well as having a relatively small on-resistance.

Functioning of MOSFETs : NMOS vs PMOS

Metal Oxide Semiconductor Field Effect Transistors, or MOSFETs, are four terminal devices (if we include the Body B), from which we use three, namely, the Gate G, Drain D and Source S. For instance, an NMOS is formed out of a p-type doped substrate (on a silicon wafer), with two small and distant two heavily doped n-type silicon (n^+). On top of the region between these n^+ layers, an insulating Oxide layer is present. The gates are connected using metal contacts. Once the gate

receives a voltage that makes its $|V_{gs}| > V_{\text{threshold}}$, then a current would flow between the source and the drain. This current flow has been possible since this applied voltage would help create a n-channel that ties the two heavily doped n+ regions. The current in the gate is always zero, since the metal-oxide-semiconductor layer is similar to a capacitor. Knowing that NMOS are activated by a high voltage and PMOS by a low one, we will call the PMOS device active low in what follows.

Designing a NOR gate using MOSFETs

We will first design a NOR gate whose output will be inverted using CMOS technology. We need two networks : one that actively sets the output to high (Pull-Up Network or PUN), and another that sets the output to low (Pull-Down Network or PDN). A NOR gate goes high when both inputs are low : this means that we need a connection to V_{cc} when both inputs are zero. This connection is established by two PMOS that are connected in series with the source of one connected to V_{cc} . For the Pull-Down Network, we need a connection to ground when at least one of the inputs is high : we chose two NMOS in parallel with the source of both connected to ground. To merge these two networks, we connect them in series as shown below.

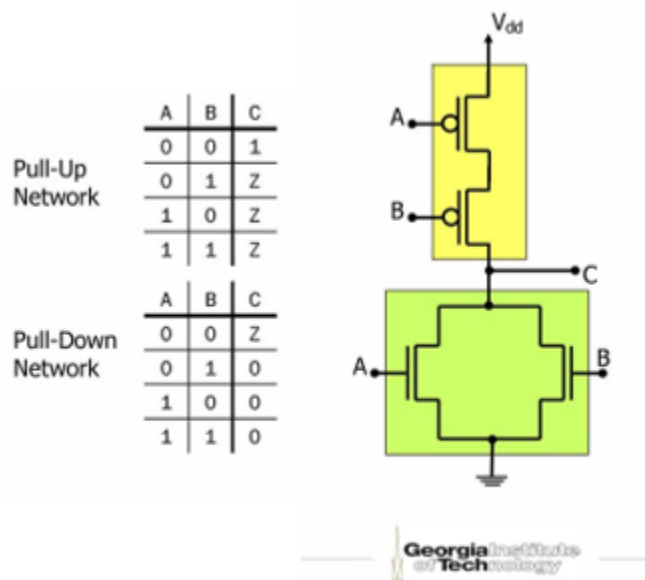


Figure 11: Pull-Up Network and Pull-Down Network for a NOR gate

Finalizing the OR Gate with a CMOS Inverter

In a similar fashion, we want a connection to V_{cc} to be established when the input is low and alternatively, a connection to ground to be established when the input is high. We will thus connect the “active-low” PMOS source to V_{cc} , the source of the NMOS to the ground and then connect their sources and gates together : this parallel-like connection would make sure that only one

MOSFET is ON at a time and thus acting like a short circuit in saturation to establish the wanted connection, either to V_{CC} or to ground. It's connection is already integrated in the IC chip

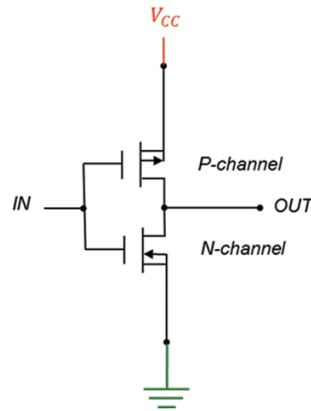


Figure 12: CMOS inverter to convert from NOR to OR gate

Connections of the HEF4007 IC

After inspecting the internal circuitry of the HEF4007 IC, we did the following connections in order to use the MOSFETs integrated on it, while using the rightmost part as an inverter directly.

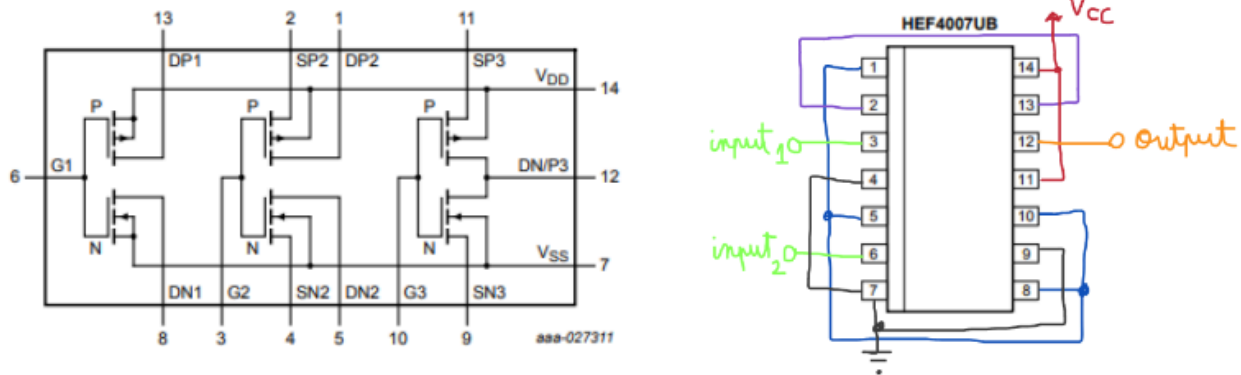


Figure 13: Internal and external connections of the HEF4007 IC

Final Detailed Schematic of the Logic OR Gate

In this design, we have chosen a V_{CC} equal to around 3 V.

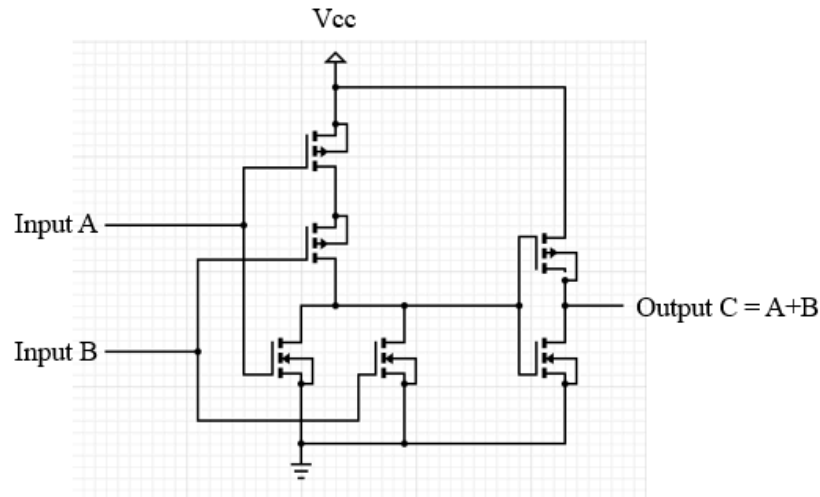


Figure 14: OR gate implementation with six MOSFETs drawn using circuit-diagram.org

Connections with Rest of the Circuit

This block takes two inputs : the output of the Heat Sensor (block I) and of the Light Sensor (block II). Its output will serve as a power supply for block IV where it turns on the sonic output device (buzzer) and closes a switch (transistor) in order to complete a DC motor circuit (block V).

Design Limitation and Optimization Recommendations

Discrete MOSFETs may have higher threshold voltages and consume more power at a given logic level than their integrated counterparts, leading to greater power dissipation and potential overheating issues in dense designs. One possible optimization that can be done is the usage of enhancement-type MOSFETs which are normally off when the gate-source voltage is zero.

IV - Sonic Output using Buzzer

Knowing that the output voltage is now designed to be high when at least one sensor is triggered, we will prepare the blocks containing the output devices, starting with the buzzer first.

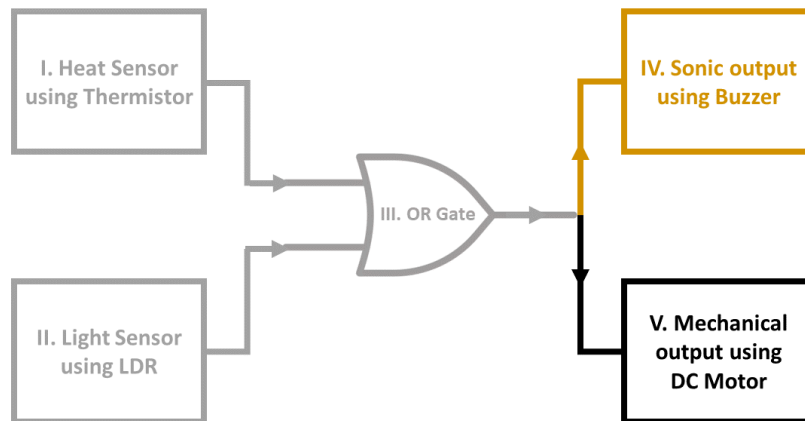


Figure 15: Reference conceptual diagram emphasizing block IV

Defining Block IV : Buzzer and Electronic Switch

The output of the OR Gate needs to be communicated to the user when needed, thus this block serves as an indicator triggered by a change in temperature or light via a sound generated by a buzzer. Also, this block will contain an electronic switch that will close in parallel with the buzzer sound. This switch will serve later to interconnect this block with that of the DC Motor (block V).

Functioning of a 3V Buzzer

A buzzer is an electronic device used to produce sound, and that operates on a low voltage, typically around 3 volts, making it suitable for battery-powered applications. Inside it exists an oscillator circuit, which comprises a piezoelectric element and other electronic components like resistors, capacitors, and sometimes a transistor. This circuit generates a continuous oscillating electrical signal (AC signal) when powered. Also, it contains a piezoelectric element, usually made of a material like lead zirconate titanate (PZT) that generates a voltage when mechanical pressure is applied; and conversely deforms when an electric field is applied. The oscillator circuit applies an alternating current (AC) to the piezoelectric disc, causing it to rapidly expand and contract. This produces vibrations in the air, which are heard as sound and whose frequency is determined by that of the electric signal, thus controlling the pitch of the sound produced. A sound is still generated when not enough voltage reaches it, but the volume would be less audible, and thus making it less convenient for an alarm circuit, similar to that we are currently aiming to design.

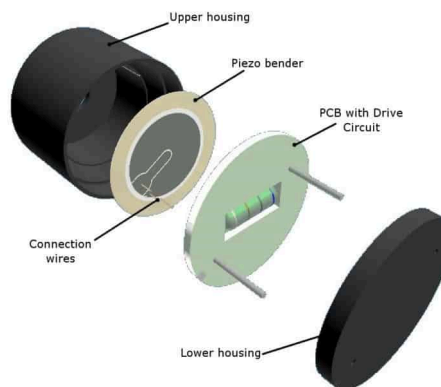


Figure 16: Internal structure and composition of the buzzer

Creating a Switch using a BJT

Before creating a switch using the BJT, we need to take a look at its structure and functioning. The structure of an NPN Bipolar Junction Transistor (BJT) consists of three layers of semiconductor material: an N-type emitter, a P-type base, and an N-type collector. Each junction forms a diode within the transistor, with the emitter-base junction and the collector-base junction being crucial for its operation. We need to bias the transistor using DC sources between the EBJ and CBJ junctions in order to make the respective “diode-like” junction either forward bias or reverse bias. It has thus three mode sof operations : cutoff when both are reversed bias, it’s in active when EBJ is forward bias and CBJ is not and in saturation when both are in forward bias.

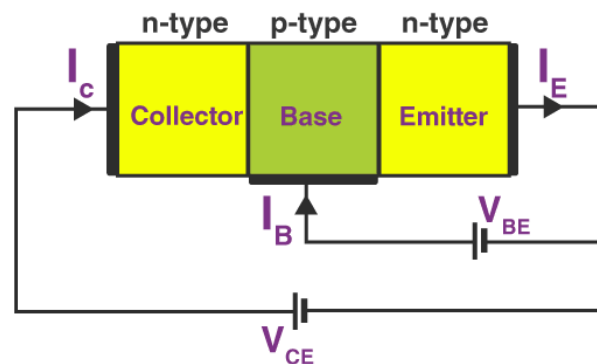


Figure 17: Structure of a npn BJT and its biasing

Creating a Switch using a BJT

The following are the three operating modes of the BJT as well as their condition in each :

- It's cutoff (C) when $V_{BE} < 0.4$
- It's active (A) when $V_{BE} \geq 0.4$ and $V_{BC} < 0.4$

- It's saturation (S) when $V_{BE} \geq 0.4$ and $V_{BC} > 0.4$

We can thus create an electronics switch using a BJT by making it go back and forth between cutoff (open circuit) and saturation (short circuit). In our case, we will make sure that the voltage at the emitter is zero, and thus the incoming voltage at the base would be higher than V_E by more than 0.7 V. Also, the 3V DC battery will be connected from the collector side, and since the voltage at the base when on would be greater than 0.4, then it's going to enter saturation right away.

Need for a Current Amplifier

Since the NMOS and PMOS transistors in the HEF4007 are not designed to handle high currents, the maximum continuous current for each transistor within the HEF4007 is limited (typically around a few milliamperes). This limitation significantly restricted the amplitude of the current output, which was also not enough to drive the DC Motor in block V although the voltage at the output of the OR gate was enough to turn on the buzzer connected between it and the ground. In order to fix this issue, we had to implement a current amplifier.

Implementing the Current Amplifier

To drive the output of the OR gate, we designed a current amplifier using an OpAmp connected to a Common Collector (CC) or emitter follower configuration using an npn BJT transistor. The property of an op-amp in a feedback arrangement is to drive its output so as to make the voltage at its inverting input equal to that at its non-inverting input. Since the non-inverting input typically will be at a certain voltage, the op-amp drives its inverting input to the same potential. The output of the op-amp is connected to the base of the NPN transistor. As the op-amp varies its output to maintain voltage equality at its inputs, this voltage drives the base of the NPN transistor. The current through the transistor (from collector to emitter) is controlled by the base-emitter voltage V_{BE} . Because the transistor's emitter is connected back to the inverting input, and thus at ground or reference voltage, the emitter current largely mirrors the base current (scaled by the beta, the current gain, of the transistor). Because of this feedback loop, any current flowing through the transistor must also flow through whatever load or additional components are placed between the emitter and the inverting input. This configuration thus converts the input current at the non-inverting terminal to a voltage across the load connected at the emitter, and it amplifies the current that can be driven through this load relative to the input current. The efficiency of this configuration lies in the fact that the output current of the emitter would be transferred as is to the "loads" since the current passing through the inverting terminal of the OpAmp is zero.

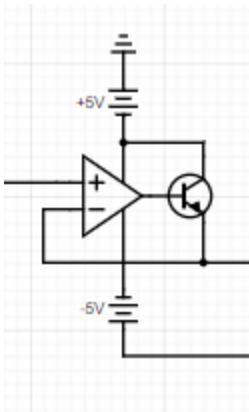


Figure 18: Current amplifier using OpAmp and BJT

Components used for the Buzzer block

- 3V Buzzer
- BJT PN2222
- Power Supply
- UA741 OpAmp

Summary of Values and Measurements

As we can see, the transistor is cut off, thus behaving like an open circuit while V_{gs} is less than V_t , that we experimentally found to be [insert threshold voltage] V. Once reached, the relation becomes linear which delimits the triode region in which I_d is proportional to V.

Table 1: Summary of values and measurements for the block

Overall Gain, Input and Output Impedances of Block IV

As we can see, the transistor is cut off, thus behaving like an open circuit while V_{gs} is less than V_t , that we experimentally found to be [insert threshold voltage] V. Once reached, the relation becomes linear which delimits the triode region in which I_d is proportional to V... We then kept on increasing the amplitude of V_{ds} until it became greater than this overdrive voltage V_{ov} .

Final Detailed Schematic of Block IV

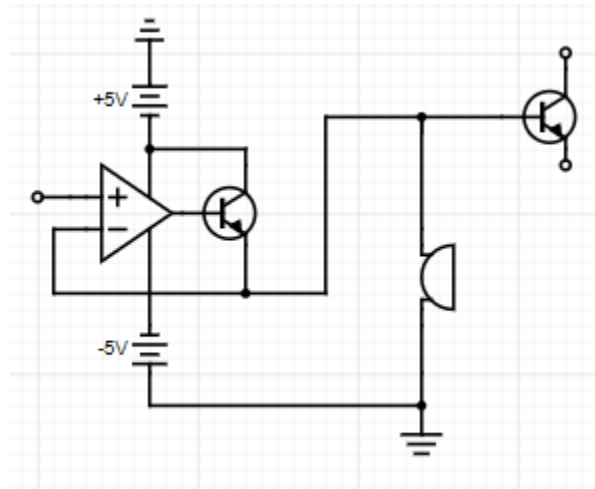


Figure 19: Current amplifier with buzzer and BJT switch

Connections with Rest of the Circuit

The transistor switch is part of a bigger circuit containing a speed regulated DC motor.

Issues encountered during Implementation

As discussed earlier, the main problem encountered during the implementation of this block was the low current from the OR gate. This was resolved via the usage of the current amplifier. Another problem was the attempt of designing a MOSFET switch instead of BJT, which even made it harder for us to foresee the current that will flow in the circuit due to the zero current at the gate.

Design Limitation and Optimization Recommendations

As we can see, the transistor is cut off, thus behaving like an open circuit while V_{gs} is less than V_t , that we experimentally found to be [insert threshold voltage] V. Once reached, the relation becomes linear which delimits the triode region in which I_d is proportional to $V_{gs} - V_t$. We then kept on increasing the amplitude of V_{ds} until it became greater than this overdrive voltage V_{ov} .

V - Mechanical Output using DC Motor

Given that the sonic output and the electronic switch have been designed, one last block needs to be connected : the mechanical response via a DC Motor with its speed controlled by a potentiometer.

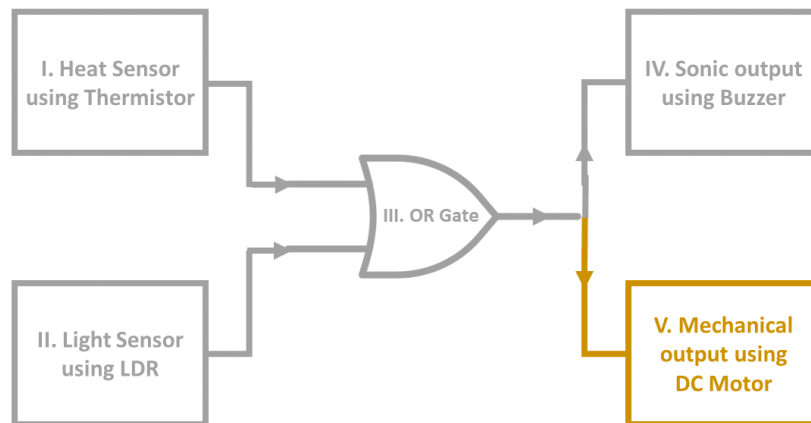


Figure 20: Reference conceptual diagram emphasizing block V

Defining Block V : DC Motor with Speed Regulator

This circuit is responsible for producing a mechanical output, namely the rotation of the DC motor that represents a door opening when one sensor is activated. It also needs to contain a speed controlling unit using a potentiometer that will be used to tune the motor's speed once ON.

Functioning of the DC Motor

A DC motor converts direct current electrical energy into mechanical energy through the interaction of magnetic fields. It comprises a stationary stator that may contain permanent magnets or electromagnetic windings, and a rotating rotor (or armature) connected to an output shaft. The rotor is equipped with windings through which DC current flows, creating a magnetic field that interacts with the stator's field. This interaction generates a force that rotates the rotor. A commutator attached to the rotor reverses the direction of current in the rotor coils during each half-turn, maintaining continuous rotational motion. The motor's speed can be controlled by varying the input voltage, and the rotation direction can be reversed by changing the polarity of the DC supply. Brushes maintain an electrical connection between the stationary and rotating parts to ensure continuous operation. This setup enables DC motors to drive various mechanical systems in multiple applications.

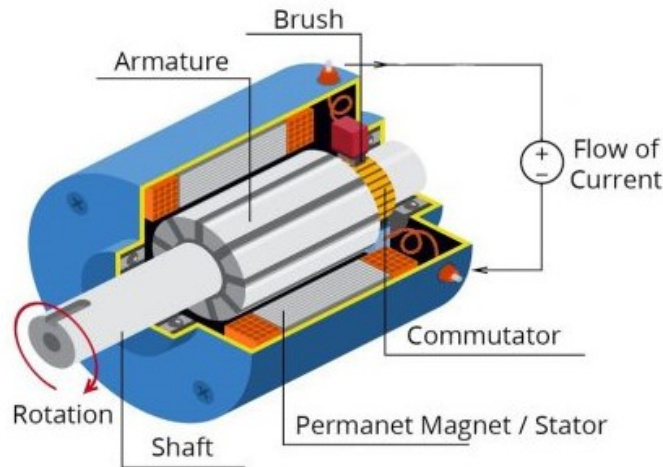


Figure 21: Internal structure and composition of the DC motor

Usage of a Flyback Diode

A flyback diode is an essential component used in circuits with inductive loads like DC motors. The primary reason for using a flyback diode is to protect other components in the circuit from voltage spikes generated by the motor, especially when the motor is suddenly switched off. Motors are inductive loads, which means that they store energy in a magnetic field around their coils when powered. When the motor is running, current flows through its windings and generates this magnetic field. If the current supply is suddenly interrupted (such as turning off the motor), the magnetic field quickly collapses. According to Faraday's law of electromagnetic induction, the collapse of the magnetic field induces a high voltage across the motor's windings in an attempt to keep the current flowing as per Lenz's Law. This phenomenon is known as inductive kickback or back electromotive force (EMF). Thus, we connect a flyback diode oriented opposing this EMF.

Functioning of the Potentiometer

A potentiometer is a variable resistor that functions as either a voltage divider or an adjustable resistor, featuring three terminals connected to a resistive element and a movable wiper. By manually adjusting the knob or slider, the wiper's position along the resistive element changes, which in turn alters the voltage across the terminals or the resistance in the circuit. We will be using it here as a speed controller. Suppose we have added a resistance instead of a potentiometer, then the voltage drop across the dc motor when the output goes high would remain the same everytime at least one of the sensors is high. Now, if we replace it by a resistance with variable resistance, such as a two-terminal rheostat or three-terminals potentiometer we can create a kind of "voltage divider" that is actually going to determine the amount of voltage the DC motor is receiving, which will consequently change its speed. We thus can control the speed of the motor once ON using a tuner.

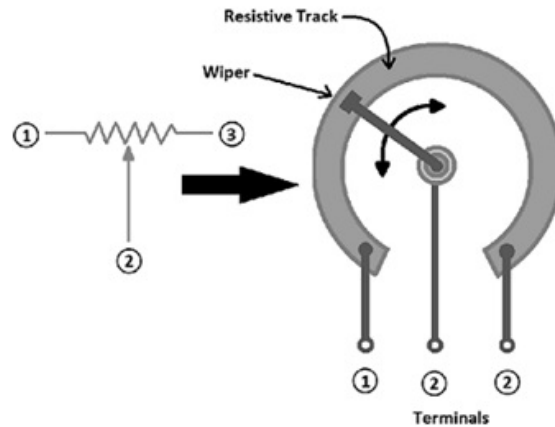


Figure 22: Internal structure and composition of a potentiometer

Components used for the motor block

- 3V DC Motor
- 1N4001 Diode
- Potentiometer

Final Detailed Schematic of Block V

As we can see, the transistor is cut off, thus behaving like an open circuit while V_{gs} is less than V_t , that we experimentally found to be [insert threshold voltage] V.

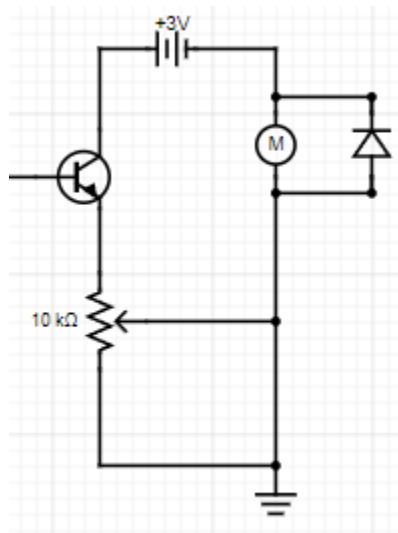


Figure 23: DC Motor Circuit controlled by a potentiometer and BJT Switch

Connections with Rest of the Circuit

This circuit is controlled by the switch implemented using MOSFETs in Block IV.

Issues encountered during Implementation

Not enough current would have been attaining the DC motor if the current amplifier in block IV wasn't designed.

Design Limitation and Optimization Recommendations

We could have used an NMOS alongside the potentiometer that has a small resistance effect when operating in the ohmic region.

VI - Connecting all Blocks Together

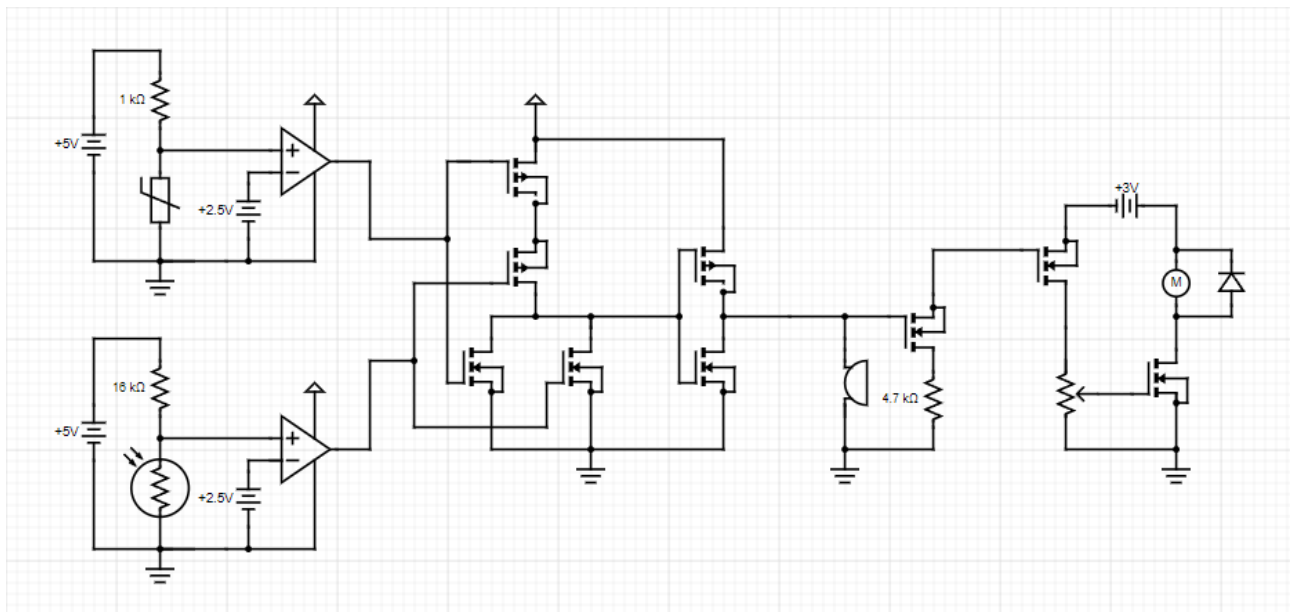


Figure 24: Final Detailed Schematic of the Dual Sensor Alarm

Conclusion

In summary, this experiment provided practical insight into the function and application of various electronic components. We utilized a comparator configuration, establishing a threshold voltage at room temperature, and monitored voltage variations in our circuit accordingly. Additionally, we employed a diode to control the circuit's openness or closure based on the voltage polarity across it. Furthermore, we utilized MOSFET transistors to construct an OR gate, enabling the activation of a buzzer and a DC motor. Moreover, we learned to amplify current across a component using an operational amplifier configuration with a transistor, crucial for powering the DC motor despite having sufficient voltage across it.

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Appendix A - Work Distribution

Circuit design : Nour (light sensor & or gate), Farah (Heat Sensor and buzzer part) & Hussam (DC motor and output circuit)

Soldering : Hussam

Report : Nour & Farah

Presentation : Nour

Appendix B - Datasheets of Used Components

Datasheet of MOSFET IC HEF4007

HEF4007UB

Dual complementary pair and inverter

Rev. 4 — 31 August 2017

Product data sheet

Nexperia

HEF4007UB

Dual complementary pair and inverter

5 Pinning information

5.1 Pinning

Figure 2. Pin configuration SO14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DP1, DP2	13, 1	drain connections from the 1st and 2nd p-channel transistors
SP2, SP3	2, 11	source connections to 2nd and 3rd p-channel transistors
G1, G2, G3	6, 3, 10	gate connections to n-channel and p-channel of the three transistor pairs
SN2, SN3	4, 9	source connections to the 2nd and 3rd n-channel transistors
DN1, DN2	8, 5	drain connection from the 1st and 2nd n-channel transistors
DN(P3)	12	common connection to the 3rd p-channel and n-channel transistor drains
Vss	7	ground (0 V)
VDD	14	supply voltage

1 General description

The HEF4007UB is a dual complementary pair and an inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors. It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2 Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B
- Inputs and outputs are protected against electrostatic effects

3 Ordering information

Table 1. Ordering information

Type number	Package	Temperature range	Name	Description	Version
HEF4007UBT	SO14	-40 °C to +85 °C	plastic small outline package; 14 leads; body width 3.9 mm		SOT108-1

4 Functional diagram

Figure 1. Logic diagram

nexperia

HEF4007UB

Product data sheet

All information provided in this document is subject to legal disclaimer

Rev. 4 — 31 August 2017

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Datasheet of Diode 1N4001

1N4001, 1N4002, 1N4003, 1N4004, 1N4005, 1N4006, 1N4007

Axial Lead Standard Recovery Rectifiers

This data sheet provides information on subminiature size, axial lead mounted rectifiers for general-purpose low-power applications.

Features

- Shipped in Plastic Bags, 1000 per bag
- Available Tape and Reel, 5000 per reel, by adding a "RL" suffix to the part number
- Available in Fan-Fold Packaging, 3000 per box, by adding a "FF" suffix to the part number
- Pb-Free Packages are Available

Mechanical Characteristics

- Case: Epoxy, Molded
- Weight: 0.4 gram (approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead and Mounting Surface Temperature for Soldering Purposes: 260°C Max. for 10 Seconds, 1/16 in. from case
- Polarity: Cathode Indicated by Polarity Band



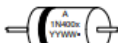
ON Semiconductor®
<http://onsemi.com>

LEAD MOUNTED RECTIFIERS
50-1000 VOLTS
DIFFUSED JUNCTION



CASE 59-10
AXIAL LEAD
PLASTIC

MARKING DIAGRAM



A = Assembly Location
1N400x = Device Number
x = 1, 2, 3, 4, 5, 6 or 7
YY = Year
WW = Work Week
• = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDEP010.

1N4001, 1N4002, 1N4003, 1N4004, 1N4005, 1N4006, 1N4007

MAXIMUM RATINGS

Rating	Symbol	1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RSM} V_{RM}	50	100	200	400	600	800	1000	V
Non-Repetitive Peak Reverse Voltage Pulsewidth, single phase, 60 Hz	V_{RSM}	60	120	240	480	720	1000	1200	V
FRMS Reverse Voltage	V_{RMS}	35	70	140	280	420	560	700	V
Average Rectified Forward Current (single phase, resistive load, 60 Hz, $T_A = 75^\circ\text{C}$)	I_{FO}	1.0						A	
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	30 (for 1 cycle)						A	
Operating and Storage Junction Temperature Range	T_J T_{STG}	-65 to +175						$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
†Indicates JEDEC Registered Data

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Maximum Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	Note 1	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS†

Rating	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage Drop, ($I_F = 1.0\text{ Amp}$, $T_J = 25^\circ\text{C}$)	V_F	0.85	1.1	V
Maximum Full-Cycle Average Forward Voltage Drop, ($I_F = 1.0\text{ Amp}$, $T_A = 75^\circ\text{C}$, 1 inch leads)	$V_{F(AV)}$	—	0.8	V
Maximum Reverse Current (rated DC voltage) ($T_J = 25^\circ\text{C}$)	I_R	0.05	10	μA
($T_J = 100^\circ\text{C}$)		1.0	50	μA
Maximum Full-Cycle Average Reverse Current, ($I_R = 1.0\text{ Amp}$, $T_A = 75^\circ\text{C}$, 1 inch leads)	$I_{R(AV)}$	—	30	μA

†Indicates JEDEC Registered Data

Datasheet of BJT PN2222

PN2222, PN2222A

PN2222A is a Preferred Device

General Purpose Transistors

NPN Silicon

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage PN2222 PN2222A	V_{CE0}	30 40	Vdc
Collector-Base Voltage PN2222 PN2222A	V_{CB0}	80 75	Vdc
Emitter-Base Voltage PN2222 PN2222A	V_{EB0}	5.0 6.0	Vdc
Collector Current – Continuous	I_C	600	mAdc
Total Device Dissipation @ $T_A = 25^{\circ}\text{C}$ Derate above 25°C	P_D	625 5.0	mW mW/ $^{\circ}\text{C}$
Total Device Dissipation @ $T_C = 25^{\circ}\text{C}$ Derate above 25°C	P_D	1.5 12	Watts mW/ $^{\circ}\text{C}$
Operating and Storage Junction Temperature Range	T_A, T_{stg}	-55 to +150	$^{\circ}\text{C}$

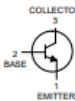
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	200	$^{\circ}\text{C/W}$
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	83.3	$^{\circ}\text{C/W}$



ON Semiconductor®

http://onsemi.com



TO-18
CASE 23
STYLE 1

MARKING DIAGRAM



PN222x Device Code
x = 2 or A
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
PN2222	TO-18	5000 Units/Box
PN2222A	TO-18	5000 Units/Box
PN2222AHLMA	TO-18	2000/Tape & Reel
PN2222AHLRM	TO-18	2000/Reel Pack
PN2222AHLRP	TO-18	2000/Reel Pack

Preferred devices are recommended choices for future use and best overall value.

PN2222, PN2222A

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 10\text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	30	–	Vdc
Collector-Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{Adc}$, $I_E = 0$)	$V_{(BR)CBO}$	60	–	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\text{ }\mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current ($V_{CE} = 60\text{ Vdc}$, $V_{CB(EB)} = 3.0\text{ Vdc}$)	I_{CXX}	–	10	mAdc
Collector Cutoff Current ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60\text{ Vdc}$, $I_C = 0$) ($V_{CE} = 50\text{ Vdc}$, $I_C = 0$, $T_A = 125^{\circ}\text{C}$) ($V_{CE} = 50\text{ Vdc}$, $I_C = 0$, $T_A = 125^{\circ}\text{C}$)	I_{CBO}	–	0.01 0.01 10 10	μAdc
Emitter Cutoff Current ($V_{EB} = 3.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	100	mAdc
Base Cutoff Current ($V_{CB} = 60\text{ Vdc}$, $V_{CB(EB)} = 3.0\text{ Vdc}$)	I_{B0}	–	20	mAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 0.1\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$) ($I_C = 1.0\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$) ($I_C = 10\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$) ($I_C = 10\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $T_A = -55^{\circ}\text{C}$) ($I_C = 150\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$) (Note 1.) ($I_C = 150\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) (Note 1.) ($I_C = 500\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$) (Note 1.)	β_{DC}	35 50 75 – 100 50 30	– – – – 300 – –	–
Collector-Emitter Saturation Voltage (Note 1.) ($I_C = 150\text{ mAdc}$, $I_B = 15\text{ mAdc}$) ($I_C = 500\text{ mAdc}$, $I_B = 50\text{ mAdc}$)	$V_{CE(sat)}$	–	0.4 0.3 1.6 1.0	Vdc
Base-Emitter Saturation Voltage (Note 1.) ($I_C = 150\text{ mAdc}$, $I_B = 15\text{ mAdc}$) ($I_C = 500\text{ mAdc}$, $I_B = 50\text{ mAdc}$)	$V_{BE(sat)}$	–	1.3 0.6 1.2 2.6 2.0	Vdc

1. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Datasheet of Thermistor NTC

NTC THERMISTOR

Introduction:

NTC (Negative temperature coefficient) thermistor is a semiconductor made from metallic oxides. It exhibits an electrical resistance that has a very predictable change with temperature. The resistance varies significantly with temperature, more so than in standard resistors. They are extremely sensitive to temperature change, very accurate and interchangeable. They have a wide temperature envelope and can be hermetically sealed for use in humid environments.


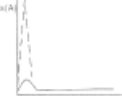
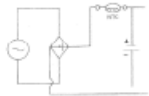
Features:

- * Longevity of service, high reliability
- * Small size, powerful, strong capability of surge current protection
- * Instant response to surge current
- * Wide operation range
- * Big material constant (B value), low remain resistance.

Application:

Thermistors are widely used as

- * Inrush current limiters
- * Temperature sensors
- * Self-resetting overcurrent protectors
- * Self regulating heating elements
- * Conversion power, switch mode power supply, UPS power protection
- * Energy saving lights, electronic ballast filament protection
- * Electronic circuit, power supply circuit protection



功率型热敏电阻元件——温度特性图

NTC THERMISTOR

How to select:

1. Maximum operating current > Actual operating current in the power loop
2. Rated zero power resistance at 25°C


$$R \approx \frac{\sqrt{2} E}{I_m}$$

Of which, E: loop voltage, Im: Surge current

For conversion power, reversion power, switch power, UPS power, Im = 100 times operating current.

For filament, heater, Im = 30 times operating current.

Marking:



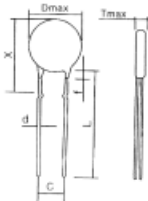
Max. Chip Diameter: Φ11mm

Diameter

Rated Zero-power Resistance: 5Ω

NTC thermistor

Dimension:



Diameter Φ	Size (mm)				
	D max.	L max.	C ± 1	T max.	d ± 0.5
5	6.5	3.1	5	4	0.55
7	8	3.1	5	4	0.55
8	9	3.1	5	5	0.7
9	10	3.1	7.5	5	0.7
10	11	3.1	7.5	5	0.8
11	12	3.1	7.5	5	0.8
13	14.5	3.0	7.5	6	0.8
15	16.4	3.0	7.5	6	1
20	22	2.9	7.5/10	7	1

* Size X depends on customer's requirement.

1/5

2/5

Datasheet of LDR

RS
Data Sheet

Light dependent resistors

NORP12 RS stock number 651-507
NSL19-M51 RS stock number 596-141

Two cadmium sulphide (CdS) photoconductive cells with spectral responses similar to that of the human eye. The cell resistance falls with increasing light intensity. Applications include: smoke detection, automatic lighting control, both counting and bargraph alarm systems.

Electrical characteristics
 $T_A = 25^\circ\text{C}$, 2954°K tungsten light source

Parameter	Conditions	Min.	Typ.	Max.	Units
Cell resistance	1000 lux 10 lux	-	400 10	-	Ω k Ω
Dark resistance	-	1.0	-	340	k Ω
Dark capacitance	-	-	3.5	-	pF
Time to 1	1000 lux 10 lux	-	2.0 10	-	ms ms
Time to 2	1000 lux 10 lux	-	40 100	-	ms ms

1. Dark to 100% R_d
2. To 10% R_d
 R_d = photoconductive resistance under given illumination.

Features

- Wide spectral response
- Low cost
- Wide ambient temperature range.

Dimensions

Light memory characteristics

Light dependent resistors have a particular property in that they remember the lighting conditions in which they have been stored. This memory effect can be minimised by storing the LDRs in light prior to use. Light storage reduces equilibrium time to reach steady resistance values.

NORP12 (RS stock no. 651-507)

Absolute maximum ratings

Voltage, ac or dc peak: 30V
Current: 75mA
Power dissipation at 25°C: 250mW
Operating temperature range: -55°C to +75°C

232-3816

Absolute maximum ratings

Voltage, ac or dc peak: 30V
Current: 75mA
Power dissipation at 25°C: 250mW
Operating temperature range: -55°C to +75°C

*Derate linearly from 250mW at 25°C to 0W at 75°C.

Electrical characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Cell resistance	10 lux 100 lux	-	100 10	-	k Ω k Ω
Dark resistance	10 lux after 24hrs	10	-	100	k Ω
Spectral response	-	-	100	-	nm
Time to 1	1000 lux 10 lux	-	20 10	-	ms ms
Time to 2	1000 lux 10 lux	-	40 100	-	ms ms

Figure 4 Resistance as a function illumination

Figure 5 Spectral response

Datasheet of DC Motor

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TECO MOTOR **Motor Specification** Page 2

2. STANDARD OPERATING CONDITIONS

ITEM	SPECIFICATION
a. Rated Voltage	DC 7.2VDC
b. Operating Voltage range	DC 5V-7.5VDC
c. No Load Current	Below 160mA
d. No Load Speed	880±10%RPM
e. Operating Environment	1. Working temperature: -30°C and +40°C Working humidity: 15%-95% RH
f. Storage Environment	1. Storage temperature: -30°C and +70°C 2. Storage humidity: 10%-90% RH (No condensation of moisture)

3. MEASURING CONDITION

ITEM	SPECIFICATION
a. Temperature	26±2°C
b. Humidity	65±5%RH
c. Motor Position	Shaft Horizontal

ALL DATA ARE BASED ON THE MEASUREMENT UNDER THE TEMPERATURE OF 25°C AND HUMIDITY 65%RH. HOWEVER, IT IS ALSO APPLICABLE AT THE RANGES OF TEMPERATURE 18-35°C AND HUMIDITY 36-95% RH.

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TECO MOTOR **Motor Specification** Page 3

4. MECHANICAL SPECIFICATION

ITEM	SPECIFICATION
a. Shaft and pin:	0.82mm-0.5mm
b. Shaft vibration	Below 0.03mm
c. Mechanical noise	64dB (max) with the following condition: No load rated voltage, motor horizontally held, measured by IEC-A (BMS) at 10cm away from metal housing on protruded shaft side. Motor should be put on the sponge as shown with the arrow downward. Background noise: 26dB

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TECO MOTOR **Motor Specification** Page 4

5. ELECTRICAL CHARACTERISTICS

ITEM	SPECIFICATION
a. Rated Voltage	7.2V DC
b. No Load Speed	880±10%RPM
c. No Load Current	Below 160mA
d. Insulation Resistance	1MΩ Min (DC 100V)
e. Testing Circuit	Testing circuit operated at 7.2V, 8Ω


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Datasheet of Buzzer

Buzzer



pro-SIGNAL

RoHS Compliant

Features

- Black in colour
- With internal drive circuit
- Sealed structure
- Wave solderable and washable
- Housing material: Noryl

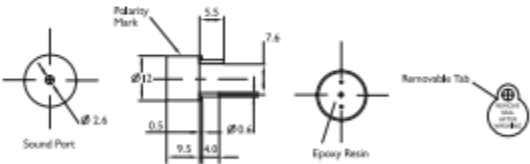
Applications

- Computer and peripherals
- Communications equipment
- Portable equipment
- Automobile electronics
- POS system
- Electronic cash register

Specifications:

Rated Voltage : 6V DC
Operating Voltage : 4 to 8V DC
Rated Current* : ≤30mA
Sound Output at 10cm* : ≥85dB
Resonant Frequency : 2300 ±300Hz
Tone : Continuous
Operating Temperature : -25°C to +85°C
Storage Temperature : -30°C to +85°C
Weight : 2g
*Value applying at rated voltage (DC)

Diagram



Dimensions : Millimetres
Tolerance : ±0.5mm

Part Number Table

Description	Part Number
Buzzer, Electromech, 6V DC	ABI-009-RC

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Datasheet of OpAmp UA741

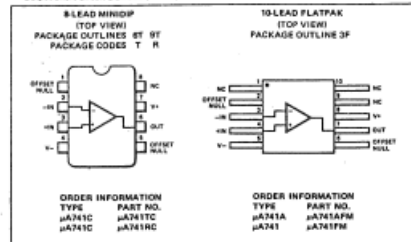
μA741 FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA741 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar[®] epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. Electrical characteristics of the μA741A and B are identical to MIL-M-38510/10/101.

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
μA741A, μA741, μA741C	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Molded and Hermetic DIP	670 mW
Mini DIP	310 mW
Flatpak	170 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	–55°C to +150°C
Metal Can, Hermetic DIP, and Flatpak	
Mini DIP, Molded DIP	–55°C to +125°C
Operating Temperature Range	–55°C to +125°C
Military (μA741A, μA741)	
Commercial (μA741E, μA741C)	0°C to +70°C
Lead Temperature (Soldering)	300°C
Metal Can, Hermetic DIPs, and Flatpak (60 s)	
Molded DIPs (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite



Notes on following pages.

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FAIRCHILD LINEAR INTEGRATED CIRCUITS • μA741

μA741A

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25^\circ C$ unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S < 50\Omega$	0.8	3.0		mV
Average Input Offset Voltage Drift			15		$\mu V/^\circ C$
Input Offset Current		2.0	30		nA
Average Input Offset Current Drift			0.5		$nA/^\circ C$
Input Bias Current		30	80		nA
Power Supply Rejection Ratio	$V_S = \pm 10, -20, 10, -10V$, $R_S = 50\Omega$	15	50		$\mu V/V$
Output Short Circuit Current	$V_S = \pm 20V$	10	25	30	mA
Power Dissipation	$V_S = \pm 20V$	60	150		mW
Input Impedance	$V_S = \pm 20V$	1.0	6.0		MΩ
Large Signal Voltage Gain	$V_S = \pm 20V$, $R_L = 2k\Omega$, $V_{OUT} = \pm 15V$	50			V/mV
Transient Response					
Rise Time			0.25	0.8	μs
Overshoot			6.0	20	%
Slew Rate (Note 4)			437	1.5	MV/s
Slew Rate (Unity Gain)	$V_{IN} = \pm 10V$		0.3	0.7	V/μs
The following specifications apply for $-55^\circ C \leq T_A \leq +125^\circ C$					
Input Offset Voltage			4.0		mV
Input Offset Current			30		nA
Input Bias Current			210		nA
Common Mode Rejection Ratio	$V_S = \pm 20V$, $V_{IN} = \pm 15V$, $R_S = 50\Omega$	80	95		dB
Adjustment For Input Offset Voltage	$V_S = \pm 20V$	10			mV
Output Short Circuit Current		10		40	mA
Power Dissipation	$V_S = \pm 20V$			165	mW
–55°C				125	mW
+125°C					
Input Impedance	$V_S = \pm 20V$		0.5		MΩ
Output Voltage Swing	$V_S = \pm 20V$, $R_L = 10k\Omega$		±15		V
$R_L = 2k\Omega$			±15		V
Large Signal Voltage Gain	$V_S = \pm 20V$, $R_L = 2k\Omega$, $V_{OUT} = \pm 15V$		32		V/mV
$V_S = \pm 15V$, $R_L = 2k\Omega$, $V_{OUT} = \pm 12V$			16		V/mV

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient dissipation linearly at 6.3mW/°C for the metal can, 8.3mW/°C for the DIP and 5.1mW/°C for the Flatpak.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.
4. Calculated value from: $BW(MHz) = \frac{Slew Rate (V/\mu s)}{2\pi \times Rise Time (\mu s)}$

*Planar is a patented Fairchild process.

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